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Effects of Load Flow on Relay Performance

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INTRODUCTION

Load flow can have an adverse effect on relay performance, but most probably the majority of applications are made and settings calculated where load flow is either assumed to be zero or considered in a cursory manner. However, there are certain relays and schemes where load flow must be comprehensively analyzed to permit a viable application. In other cases load flow may be neglected and the relay system will perform properly until a contingency situation arises that causes an incorrect relay operation attributable to the effects of load flow. This paper will discuss several relay types and application situations for transmission line protection where load flow must be considered. In some cases the application restrictions imposed by the load flow are simply pointed out. In other cases design innovations in recently introduced relays are described that mitigate the adverse effects of load flow.

Throughout this paper reference will be made to variations of the representative system shown in *Figure 1*. All system impedances are assumed to be pure reactance (90°), and the impedances are given in per unit. As will be pointed out in the following sections, the Z_S/Z_L ratio can be a critical parameter in analyzing the response of relays when load flow is considered. *Figure 1* shows a system where the source to line impedance ratio, Z_S/Z_L, is relatively low. The source voltages are designated as E_L and E_R. where (L) indicates left and (R) indicates right. The left / right designation is used to indicate load flow direction. The load magnitude is specified by the angular separation between the left and right source voltages. Consequently, the specification, 30° L-R, indicates left-to-right load flow while 60° L-R indicates the same direction but approximately double the magnitude.

DISTANCE RELAYS

An ideal distance relay sees an apparent impedance equal to the positive sequence impedance from the relay location to the fault location. There are many factors that conspire against a realization of such an ideal distance relay. Load flow coupled with fault arc resistance / ground fault impedance can result in overreach for line-end faults and incorrect directional action for close-in reverse faults.

Combined Effect of Load Flow and Ground Fault Resistance

A previous paper[1] described the effects that load flow has on mho ground distance relay performance. Load flow affects distance relay performance in two ways. First the apparent impedance is altered because of the load flow in combination with fault resistance / impedance. Secondly the load flow causes a shift of the distance relay characteristic as plotted on an R-X diagram.

Figures 2 and 3 show the apparent impedance locus for a compensated ground distance relay at the left bus of the system in *Figure 1*. A compensated ground distance relay is one where the apparent

impedance for phase A is:

$$Z_R = V_{AG} / I_R$$

where: $I_R = I_1 + I_2 + K_0 I_0 = (I_A - I_0) + K_0 I_0$
$K_0 = Z_{0L}/Z_{1L}$
Z_{0L} = zero sequence impedance of the line
Z_{1L} = positive sequence impedance of the line

If K_0 exactly equals the Z_{0L}/Z_{1L} ratio (in magnitude and phase angle) and the fault resistance is zero, the relay will see the actual positive sequence impedance to the fault.

With the fault resistance greater than zero ($R_F>0$) the apparent impedance deviates from the actual positive sequence impedance. *Figure 2* plots the relay apparent impedance locus for $0< R_F< I$ at 15° L-R and 30° L- R load flow. Note that as R_F approaches infinity the apparent impedance approaches the load impedance point. *Figure 2* graphically illustrates the potential for first-zone relay overreach with a line-end phase-to-ground fault.

The type of relay characteristic used will determine whether or not an overreach problem exists. Mho ground distance relays using the proper polarizing quantity exhibit system dependent and load flow dependent characteristics which tend to prevent overreach for the above condition while providing enhanced coverage in the 1st quadrant of the R-X diagram as compared to mho relays whose characteristic is a circle that plots through the origin of the R-X diagram.[1] Negative sequence current polarized reactance relays eliminate the possibility of overreach for the above condition – assuming a homogeneous system – as compared to conventional reactance or quadrilateral relays that will overreach.[2] Both of these points were covered in detail in previous papers.

Figure 3 plots the relay apparent impedance locus for $0<R_F<7$ at 30° R-L load flow. Here the load flow direction has been reversed and the internal A-G line fault is at the left bus, the relay location. It is quite apparent from *Figure 3* that the impedance locus forms a circle. Actually, the plots in *Figure 2* are arcs of circles, but this is not readily apparent. *Figure 3* indicates that the selected first-zone relay characteristic must have a large 1st quadrant coverage to see high resistance phase-to-ground faults directly in front of the relay.

Directional Action for Close-in Reverse Faults

Certain designs of phase distance and ground distance relays are susceptible to incorrect operation for close-in reverse faults. Load flow in a particular direction can increase the likelihood of such an incorrect operation. Consider a simple mho phase relay using a two input comparator as shown in *Figure 4*. The measuring unit shown is for phase pair A-B, and it utilizes a phase angle comparator that requires 90° or more of coincidence between phasors (I_A-I_B) Z_R-V_{AB} and V_{AB} before an output is permitted.

For the simple radial case as shown in *Figure 5*, a reverse direction phase-to-phase fault is assumed just behind the relay location. If the angle of the source plus line impedance is 85°, the fault current

lags the source voltage by 85°, and the arc drop (voltage at the relay location) also lags the source voltage by 85°. The current through the relay is 180° from the arc drop, and IZ_R – assuming an 85° relay replica impedance – is 180° from the source voltage. V_{OP} differs from IZ_R by the arc drop voltage.

As shown in the phasor diagram of *Figure 5*, the angle between V_{OP} and the initial polarizing voltage is approximately 165°. As the memory action decays, the polarizing voltage shifts lagging to the steadystate (V_{ARC}) position, giving a final steady-state angle that is smaller but still greater than 90°. Therefore the relay has less tendency to operate under the dynamic (initial) condition than it does steady-state, but it does not operate under either condition.

Figure 6 shows the effect of load flow in the tripping direction with the conditions depicted on the one-line diagram. For the relay at the far left bus and a phase-to-phase fault directly behind it the relay current is driven by a voltage that lags the initial polarizing voltage. As a result, both the dynamic and steady-state angles between V_{OP} and V_{POL} are considerably more than 90°, and the relay does not operate.

Figure 7 shows the effect of load flow in the non-tripping direction for the same conditions as in *Figure 6*. This is accomplished by placing the relay at the far right bus. For a phase-to-phase fault directly behind the relay, the driving voltage for the fault current now leads the initial polarizing voltage, and IZ_R is shifted leading by approximately 60° compared to its position in *Figure 6*. The dynamic angle is much greater than 90°, a non-trip condition, but the steady-state angle is slightly less than 90° and could produce a trip output if the arc voltage is above the sensitivity level of the polarizing circuit. More recent designs of mho phase relays add a portion of the positive sequence voltage to the polarizing quantity, $V_{AB} + K_{VAB1}$ in this case, which provides more security against false tripping on close-in external phase-to-phase faults under adverse load flow conditions.[3]

Mho ground distance relays utilizing a simple two-input phase angle comparator are susceptible to incorrect operation for close-in reverse phase-to-ground and phase-phase-to-ground faults. Instruction books for this type of ground distance relay have always contained a caution and calculation procedure to assure that the forward reach is not set so large as to cause the relay to operate incorrectly on reverse ground faults. However, the suggested calculation procedure assumed no load flow. It has been demonstrated[4] that load flow combined with adverse system impedances can result in such relays operating incorrectly for this condition even though the suggested calculation procedure indicates otherwise. A recent memo[5] distributed by General Electric suggests a method for checking such applications that takes into account the load flow effects.

More recent static designs of mho ground distance relays incorporate multi-input (more than two) phase angle comparators that virtually eliminate the possibility of incorrect operation for a close-in reverse ground fault.[6] In essence this is accomplished by two of the comparator inputs producing a zero sequence directional unit that supervises the mho unit.

Phase Selection by Distance Relays

In general, the source to line impedance ratio determines the ease of obtaining correct phase selection in applications involving single pole tripping and reclosing. With large source to line impedance ratios, phase selection is very simple since it can be shown that only one of the ground distance relays responds to single-line-to-ground faults, only the phase distance relays respond to phase faults, and the phase relays do not respond to single-line-to-ground faults.

As the source to line impedance ratio decreases, the unfaulted-phase relays will begin to operate for internal faults. For example, it is well known that phase relays will operate for close-in single-line-to-ground faults, requiring some form of ground preference to prevent phase relay operation from initiating a three pole trip. Further, the problems of correct phase selection are aggravated by heavy load flow and, in some cases, by a low ratio of zero sequence to positive sequence source impedance. The following examples of problem areas are based on the equivalent system of *Figure 1* with the relay location at the left bus and load flow in the tripping direction (i.e., L-R).

1. Close-in single-line-to-ground fault with fault resistance.
   This case assumes a phase-A-to-ground fault directly in front of the relay location. *Figure 8* plots the compensated impedance seen by the phase C ground distance relay. The fault resistance is assumed to be 0.5 p.u. and the data points indicate the different load flow angles. As the load flow increases, the probability of phase C relay operation increases.

2. Remote single-line-to-ground fault without fault resistance.
   This case assumes a bolted phase-A-to-ground fault at the remote end of the line with increasing load flow in the tripping direction. *Figure 9* plots the compensated impedance seen by the phase C ground distance relay for the different load flows. Note that as the load flow increases the probability that the phase C relay will operate is significantly increased. The effect of adding fault resistance would be to make the phase C relay less likely to operate.

3. Phase relay operation on remote single-line-to-ground fault.
   All conditions are the same as for case (2) above but *Figure 10* plots the impedance seen by the C-A phase distance relay with different load flow magnitudes. It is interesting to note that phase C-A relay may be even more likely to operate than the phase C relay, with a significant tendency to overreach. The effect of adding fault resistance would be to make the phase C-A relay slightly more prone to operate.

4. Ground relay on remote phase-to-phase fault.
   This case assumes a bolted phase B-C fault at the remote end of the line, and *Figure 11* illustrates the compensated impedance seen by the phase B and phase C ground distance relays. Note that the phase B ground relay has a similar tendency to operate on a phase-to-phase fault as the phase relay does on a single-line-to-ground fault. Thus a ground distance relay preference is not a complete solution to the problems of correct phase selection. *Figure 11* also illustrates that the phase C ground distance relay tends to underreach in contrast to the overreach of the phase B relay.

In general, the severity of the problem of incorrect phase selection in the above cases will be a function of the type and shape of the relay characteristic and the reach settings employed. As noted previously, an increasing source to line impedance ratio will reduce the probability of having phase selection problems. There may be other cases that will result in incorrect phase selection. For example, the phase A-B relay sees an impedance that crosses the X axis from quadrant II to I as a phase-A-to-ground fault is moved along the line during load flow in the tripping direction. Thus using a minimum area characteristic on the R-X diagram is not a complete solution to the problem.

Performance With One Pole Open — Single Pole Tripping

In single pole tripping schemes the ground distance units must provide correct distance measurement when a pole is open as well as when all three phases are in service. The dissymmetries associated with an open phase affect not only the relays on the line with the open pole, but they also affect the performance of the relays on adjacent lines. Consider the system shown in *Figure 12*. Phase B is open in a line section between the protected line and the source at the right. A phase B-C fault is applied on the right bus at the end of the protected line. Assume that the zone one relays at the left bus are set for 90% of the positive sequence impedance of the line with the zero sequence current compensation (K_0) set to 3. The relay and system angles are all 90°.

Table 1 shows the operate signal, polarizing signal, and coincidence angle for a simple mho ground distance unit utilizing a two-input phase angle comparator. Case 1 is a B-C fault with no load flow; case 2 is a B-C fault with 15° L-R load flow. With no load, the phase B unit is almost at its balance point. With load, the first zone phase B unit overreaches and operates for the external phase-to-phase fault. Note that due to the low Z_S/Z_L ratio at the left, the polarizing voltage will not change substantially regardless of the type of polarizing used (i.e.. unfaulted phase, faulted phase, positive sequence, quadrature).

Table 2 is similar to Table 1 except that a zero sequence reactance unit is evaluated. This reactance relay overreaches for the phase-to-phase fault even without load flow. The apparent impedance seen by the phase B relay for the B-C fault, with and without load flow, is shown on an R-X diagram in *Figure 13* along with representative mho, reactance, and quadrilateral characteristics. More recent designs of mho ground distance units, as found in the TLS relay system, avoid incorrect operations for these conditions by using multi-input phase angle comparators with adjustable sensitivities on the various inputs.

Multi-Zone Relaying

Faults beyond the remote end of the line produce apparent impedance loci similar to those produced with a combination of load flow and fault resistance as discussed previously. The load flow imparts an apparent phase shift to the fault impedance and impedance magnification results from in-feed from the remote end of the line. *Figure 14(b)* illustrates the impedance locus seen by a phase A ground distance relay for a phase-A-to-ground fault on the system in *Figure 14(a)* with R-L load flow and L-R load flow.

If a distance relay is to detect this remote external fault it should have a relatively large circular characteristic. However, such a characteristic will tend to operate on heavy load flow. Thus the application of third zone distance relays on long transmission lines becomes very difficult and, as a consequence, negative or zero sequence overcurrent relays are increasingly preferred for backup protection.

Out-of-Step Blocking

The use of phase distance relays to implement an out-of-step blocking scheme on lines equipped with three pole tripping is well established. Traditionally a single phase measuring unit is utilized and the scheme output blocks all three phases of protection. However, in applications where single pole tripping and reclosing is used the use of a single phase out-of-step blocking unit may significantly compromise the performance of the relay system during out-of-step or a severe load swing when one pole is open.

If the single phase unit is connected phase A to phase B, and either phase A or phase B is open, then the voltage on the open pole due to electromagnetic and electrostatic coupling will distort the impedance seen by the relay. For this reason the phase to phase relays associated with the open pole are often taken out of service when a pole is open. The impedance seen by a phase to phase unit connected to the two phases left in service will see the correct impedance undistorted by the voltage on the open pole, but it will normally not coordinate with the ground relays associated with the two intact phases. Because the zero sequence line impedance is typically 3 to 4 times the positive and negative sequence line impedances, the negative sequence current in the line with one pole open is generally much larger than the zero sequence current. The large ratio of I_2/I_0 causes dissymmetry in the two phase currents as shown in *Figure 15*. With phase A open and load in the tripping direction, *Figure 15* shows the phase B current leading the phase B voltage and phase C current lagging the phase C voltage. Thus the phase C to ground distance unit will be the first to operate, the phase B-C unit next, and the phase B to ground unit last. Correct out-of-step blocking would be assured if the out-of-step measuring unit was connected phase C to ground. However, since any phase can be open, optimum performance can be achieved by applying a phase to ground connected out-of-step measuring unit to all three phases. The TLS modular relay system incorporates an out-of-step scheme that utilizes both phase and ground distance units.

Loss of Potential

Distance relays can be affected by the loss of potential during periods of load flow, but the following factors must be considered to determine what the overall effect will be.

1. The design of the relay and the settings placed on it (reach, angle, characteristic timer, etc.).
2. The magnitude and direction of load flow
3. The nature of the potential loss (full or partial)
4. The potential transformer/CCVT connections and the total connected burden

To determine the effects of the above factors, it is necessary to examine each type of distance function separately. The following will provide detailed analysis for a mho phase function only. Similar procedures can then be used to examine other designs.

A simple mho phase function as shown in *Figure 4* is assumed. For a circular characteristic operation will occur when the angle between the polarizing and operating quantities is less than 90° (i.e., the amount of coincidence between the polarizing and operating phasors is greater than 90°). The characteristic and relevant phasors are shown in the (I)R-(I)X diagram of *Figure 16*. For the assumed function the polarizing quantity is equal to the voltage of the phase pair that the function is assigned to protect. To provide improvements in performance it is desirable to use a polarizing quantity other than the phase pair voltage alone. The positive sequence voltage – referenced to the phase pair being protected – can be used as a reliable polarizing quantity. Other designs may use a polarizing quantity made up of the voltages associated with the unfaulted phase(s). The term "cross-polarized" is often used to refer to this type of polarizing.

One way to determine the effect of potential failure is by phasor analysis. This will be done for the design shown in *Figure 4* and for a design that uses only the positive sequence voltage referenced to the same phase pair as the polarizing quantity. The A-B function will be considered in both cases. The following assumptions are made:

1. Load flow is at unity power factor.
2. The PT secondaries are connected wye-grounded and each phase is fused through a common disconnect as shown in *Figure 17*.
3. The only connected burden is the A-B, B-C and C-A voltage coils of the subject relay.
4. The mho function has memory in the polarizing circuit as shown in *Figure 4*.
5. The mho function is set with a circular characteristic.

Consider first the case where all potential is lost by an inadvertent opening of the disconnect. For this condition, the operate signal becomes IZ alone due to the loss of potential, but the polarizing voltage does not go to zero immediately due to the memory circuit. The phasor diagrams for this condition are shown in *Figure 18*, and indicate that the function will produce a momentary output – equal to the memory circuit decay time – for this condition. Notice that lagging load angles will tend to aggravate the condition, but leading load angles will tend to make the condition less onerous. The phasor analysis of *Figure 18* is valid regardless of the type of polarization utilized. It is possible to lessen the tendency to trip by making the characteristic lenticular (i.e., setting A>90° in *Figure 4*) or by applying a lagging phase shift to the polarizing voltage. The more conventional solution of supervising the distance function with an overcurrent function set above the maximum possible load current will completely eliminate any operation.

Now consider the case in which the fuse in the "A" phase circuit blows. The B-C function will have normal voltage maintained, but because of the connected burden the A-B and C-A functions will have their voltages reduced to half-normal and phase shifted 60° in the leading and lagging directions respectively. The effect of this reduction and phase shift in the voltage is shown in the phasor diagrams of *Figure 19* which clearly show that the positive sequence polarized function offers a significant improvement in performance over the function using the phase-pair voltage alone for polarization.

CURRENT DIFFERENTIAL RELAYS

A current differential relay scheme is generally defined as one that compares the currents at each terminal of a protected element to determine whether a fault is internal or external to the zone of protection. Phase comparison schemes do this by utilizing only the phase angle component of the comparison quantity. A "true" current differential scheme utilizes both the magnitude and phase angle information contained in the comparison quantity. Consequently, phase comparison relaying can be thought of as a subset of current differential relaying.

There are many types of phase comparison schemes, but the following will be limited to a discussion of a "mixed excitation" phase comparison scheme. Mixed excitation is a term used to describe a phase comparison scheme that mixes the outputs of different sequence networks in a given proportion and phase angle, and then performs the phase comparison function for *all* types of faults based on the resulting single phase quantity. There are innumerable combinations of sequence quantities that satisfy the above definition. Since there is a positive sequence component for all fault types, we could attempt to use pure positive sequence as the comparison quantity. However, this is not acceptable in most applications because of the presence of through load current during an internal fault. The phase position of the load component relative to the fault component depends on such factors as the direction of the load flow, power factor of the load, the angles of the system impedances, and which phase or phases are faulted. The phase position of the net positive sequence current – load plus fault – entering one end of the line relative to that entering the other will depend on these same factors plus the relative magnitudes of the fault and load components of current. The fault current for a three phase fault is pure positive sequence, and it generally predominates over the through load current. However, the positive sequence component of fault current for a phase-to-ground fault can be significantly less than the through load current.

In general, the heavier the fault current and the lighter the load current, the more suitable would be the use of pure positive sequence for phase comparison. Since pure positive sequence would be practical in only a minority of applications, it is not considered suitable in a scheme for general application. General Electric phase comparison schemes have successfully utilized a single-phase mixed-excitation comparison equal to:

$$I_2 - I_1/K$$

where: K = 5, 7 or 10

For such schemes the maximum phase angle between the comparison quantity at all terminals of the line for any internal fault, regardless of type or combination of phases, must be small enough to assure tripping with adequate margin. The criteria that has been established for reliable tripping is no more than 60° separation. In a "straight" phase comparison scheme in which overcurrent level detectors, operating on the same $I_2 - I_1/K$ signal, are used to control the channel keying and comparison logic, applications are limited to lines where the minimum three phase fault current is higher than maximum load. How much higher will depend upon the type of channel involved and whether the protected line has two or three terminals.

If it were possible to eliminate the load component of positive sequence current in $I_2 - I_1/K$, phase comparison schemes as described above would be more generally applicable. By the use of innovative circuit techniques, this has been accomplished in the DLS2000 line protection relay system. However, the DLS2000 is a true current differential scheme not a phase comparison scheme. As mentioned previously, the distinction between a current differential scheme and a phase comparison scheme, using the same comparison quantity, is that the current differential scheme retains the magnitude information in the comparison quantity while the phase comparison scheme discards it. Note that *under ideal conditions* a current differential scheme is in essence an implementation of Kirchoff's law (i.e., the phasor sum of all the currents entering a circuit should be a zero unless an additional current path – a fault – is added whose current is not included in the phasor sum). Under the same, but not ideal, conditions a current differential scheme is more dependable and secure than a phase comparison scheme. As an example of increased dependability, consider the case of a two terminal line where one end has a strong source and the other end a weak source. For an internal fault combined with through load, the comparison quantity at the weak source end will be essentially load current while at the strong source end it will be essentially fault current. The angle between the comparison quantities may approach 90°. This would prevent operation at either terminal for most practical phase comparison schemes. However, a current differential scheme would have ample operating energy at the strong source end, and it would, at least, produce a trip at that end.

The "load memory" circuit incorporated in the DLS2000 is shown in simplified form in *Figure 20*. The summing amplifier adds I_1 and I_1 phase shifted 180° such that the ΔI_1 output is zero for steady state conditions. When a fault occurs the filter "remembers" the prefault I_1 value forcing the transient output to be:

$$I_1 \text{ (total)} - I_1 \text{ (load)} = \Delta I_1$$

where: ΔI_1 is essentially the fault component of positive sequence current

The DLS2000 comparison quantity is $I_2 - K'\Delta I_1$, and it is designed to operate within the time that the Q of the filter in *Figure 20* will maintain the ΔI_1 output as essentially the fault component of positive sequence current. The transient output of the "load memory" circuit permits tripping for internal three phase fault current magnitudes down to approximately one-half the tap setting without loss of security under steady state load conditions. The above description is not intended to comprehensively explain the operation of the DLS2000; it merely indicates the approach taken to mitigate the adverse effects of load flow in this design.

DIRECTIONAL OVERCURRENT RELAYS

Dissymmetries in the transmission system may affect the performance of directional relays which use zero and negative sequence quantities. The dissymmetries may arise from an open pole due to normal operation of a single pole trip scheme, untransposed lines, or unbalanced load current. The performance of negative sequence and zero sequence directional units using simple (uncompensated) phase angle comparators will be considered.

The assumed system is shown in *Figure 21*. The first two cases studied assume an open pole with 15° L-R load flow and the relay potential source located on the line side of the circuit breaker. The coincidence between the operate (IZ) and polarize (V) quantities is shown in Table 3. When the coincidence angle is 90° or greater, the associated directional unit will operate.

For case 1, both directional units – negative and zero sequence – at the right end will be picked up for the assumed load condition, but neither unit will operate at the left end. When a phase-B-to-ground fault occurs at the right end, as in case 2, the directional units at the right end remain picked up and, at the left end, the coincidence decreases from case 1. Therefore the directional units at the left end will not see the B-G fault at the remote end, and a directional comparison blocking scheme using zero or negative sequence directional units would not operate.

If the relay potential source is located on the bus side of the circuit breaker rather than on the line side, both the negative and zero sequence directional units, at both ends, will be operated under load as shown in case 3. All units will also operate during a B-G fault as shown in case 4. With bus side potential both the dissymmetry of the open pole and the fault are internal to the relay; this is not the case when line side potential is employed. When the dissymmetry is internal – whether due to a fault or other cause – the sequence directional units will tend to operate. With line side potential the performance of the negative and zero sequence directional units varies with system conditions. Because of this, single pole tripping schemes are generally arranged such that any negative or zero sequence directional units are taken out of service during the open pole period.

While many systems do not employ single pole tripping, the directional units may still be affected by existing dissymmetries such as those caused by untransposed lines. The performance of the directional units on untransposed lines is similar to their performance on lines with an open pole and bus side potential. That is, for load conditions the directional units at both ends of the line will tend to operate indicating an internal fault. If the associated overcurrent units were set sensitive enough to operate on this unbalance, a false trip would result. However, it is not sufficient that the overcurrent unit be set to not operate on the unbalance due to load. The same situation could be caused by an external three phase fault.

In general, negative and zero sequence overcurrent units are sensitive to unbalances in the presence of load current or external three phase faults, and the settings must be raised accordingly. Several of the overcurrent units in General Electric relays use positive sequence current restraint to eliminate this problem. For example, in such negative sequence units the operate current is $|I_2| - K|I_1|$. A portion of the positive sequence current is subtracted from the negative sequence current. As the load current increases, the unit is automatically desensitized, but it is still sensitive to low level faults during low load conditions. A unit of this design is used in the SLYP/SLCN relay equipment enabling it to achieve superior performance on high resistance ground faults.

CONCLUSION

The effects of load flow on relay performance have been discussed in a rather selective manner. Only transmission line protection has been considered, but even with this restricted scope it can be seen that load flow has the potential for dramatically altering the performance of many common relay measuring functions and schemes.

The extent to which the performance is affected depends upon the design of the particular relays utilized and whether the settings employed are based on an evaluation of the effects of load flow. The manufacturer can, by the use of innovative circuit design, mitigate the adverse effects of load flow. The manufacturer should supply sufficient application information to permit the user to evaluate the effects of load flow on a particular relay or scheme. The user should make use of this information and combine it with good engineering judgment to implement a secure and dependable application.

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TABLE 1

$V_{OP} = (I_B - I_0)Z_{R1} + K_0I_0Z_{R0} - V_{BG}$
$V_{POL} = V_{BG}$

case	1	2
load	0°	15° L-R
V_{OP}	.55 $\angle$-25.3	.49 $\angle$-32.6
V_{POL}	1 $\angle$-120	1 $\angle$-120
coincidence	85.3°	92.6°

TABLE 2

$V_{OP} = (I_B - I_0)Z_{R1} + K_0I_0Z_{R0} - V_{BG}$
$V_{POL} = I_0X$

case	3	4
load	0°	15° L-R
V_{OP}	.55 $\angle$-25.3	.49 $\angle$-32.6
V_{POL}	.1 $\angle$-90	.1 $\angle$-105.6
coincidence	115°	107°

TABLE 3

Case 1: 15° L-R load flow
line side potential
no fault

Case 2: 15° L-R load flow
line side potential
B-G fault at F1

Case 3: 15° L-R load flow
bus side potential
no fault

Case 4: 15° L-R load flow
bus side potential
B-G fault at F1

case	Directional Unit Coincidence (Degrees)			
	Left Relay		Right Relay	
	Neg.	Zero	Neg.	Zero
1	71	70	96	95
2	38	51	134	97
3	180	170	180	170
4	180	170	180	170

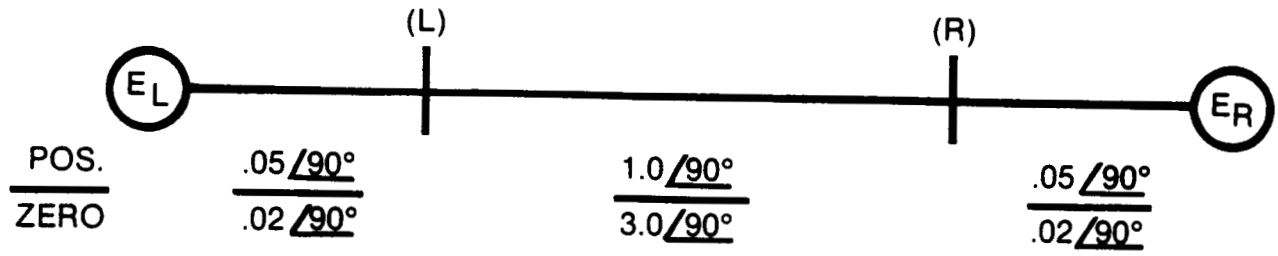


Figure 1. Representative System One-Line Diagram

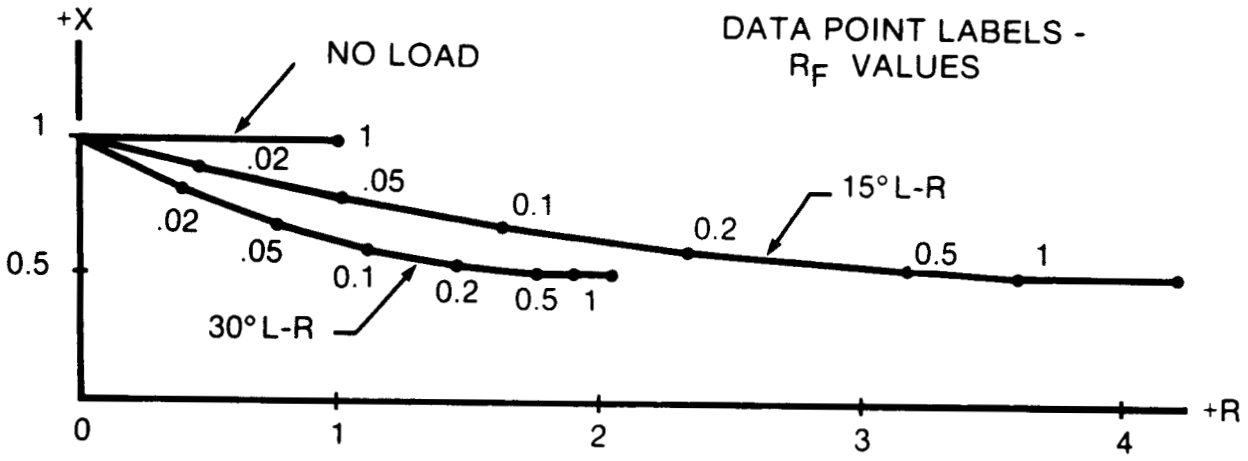


Figure 2. Compensated Impedance Seen by Phase A Relay for A-G Fault at Line-End (L-R Load Flow)

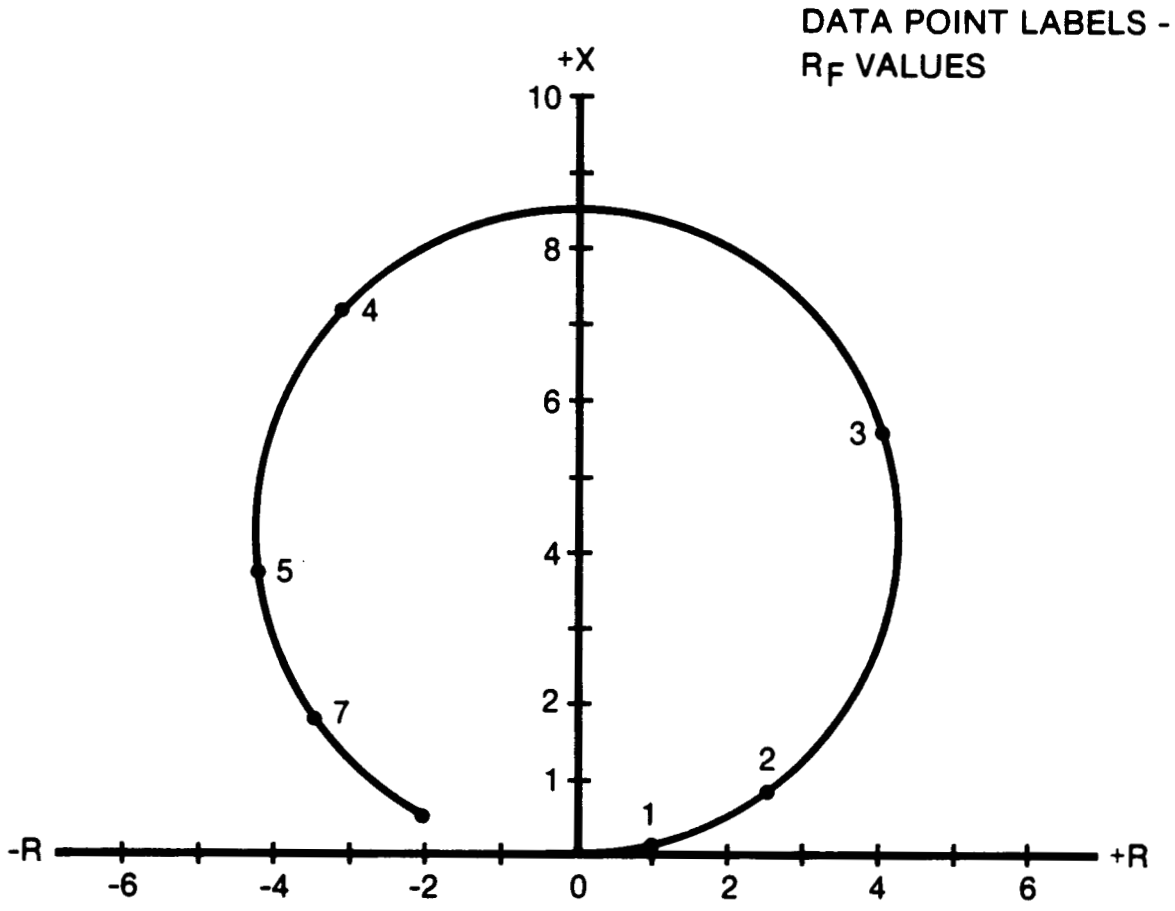


Figure 3. Compensated Impedance Seen by Phase A Relay for A-G Fault at Relay Location (R-L Load Flow)

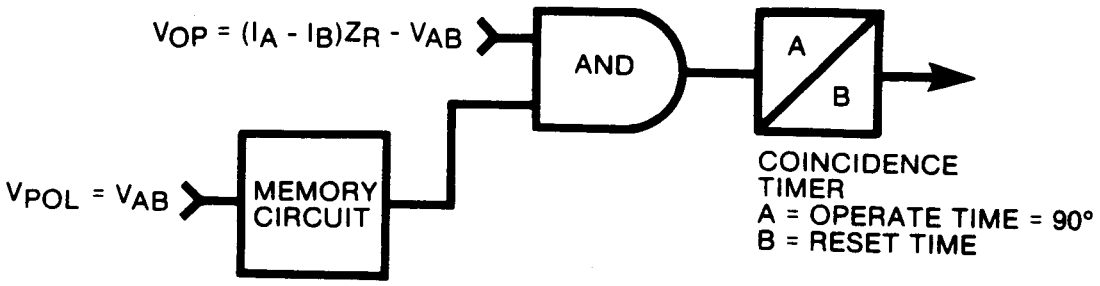


Figure 4. Phase Angle Comparator Mho Distance Relay for the AB Phase Pair

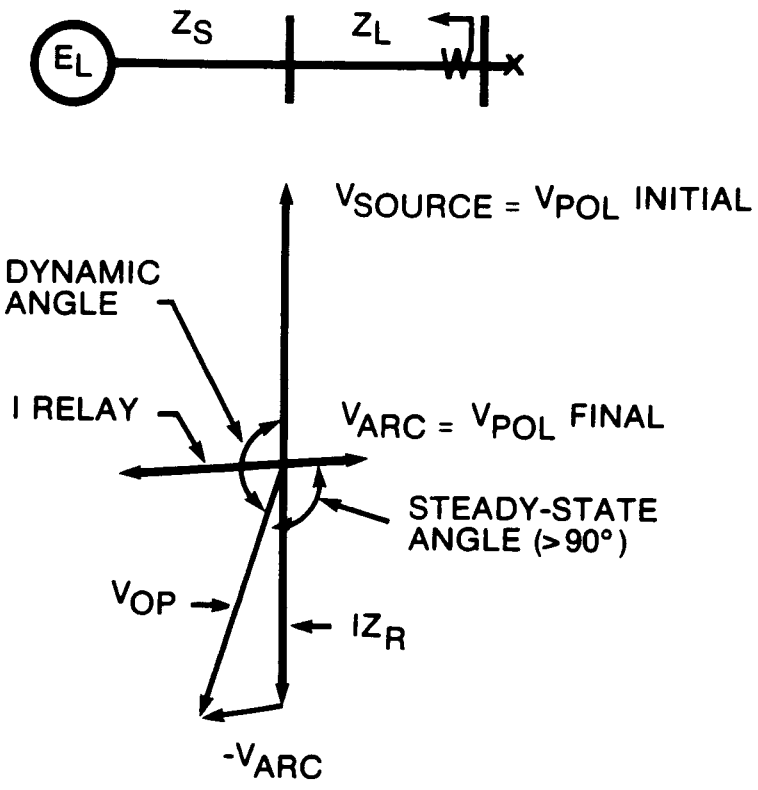


Figure 5. Polarizing and Operating Phasors for Reverse Direction Fault, Radial Feed

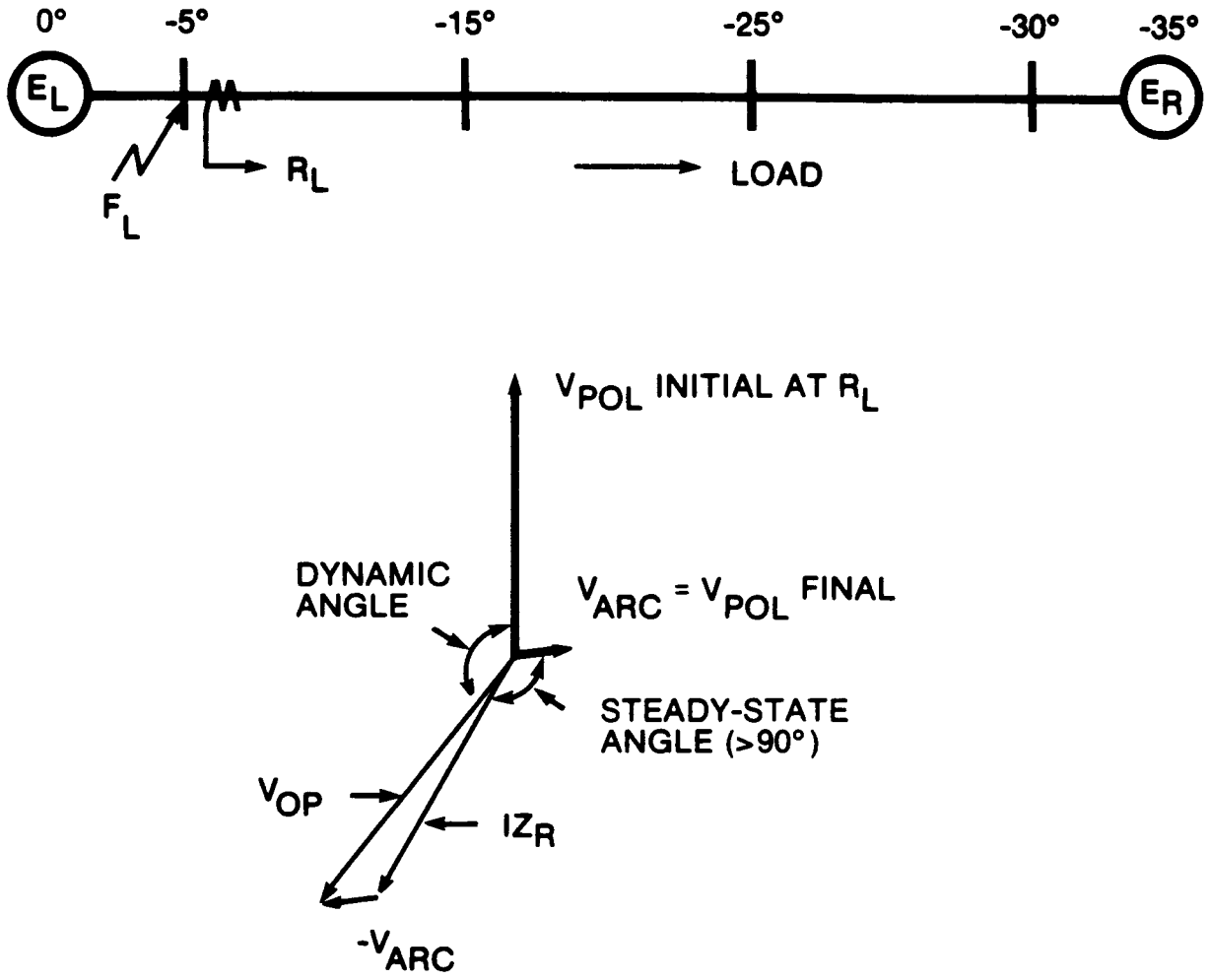


Figure 6. Phasors for R_L Relay and F_L Fault, Load Flow in Tripping Direction

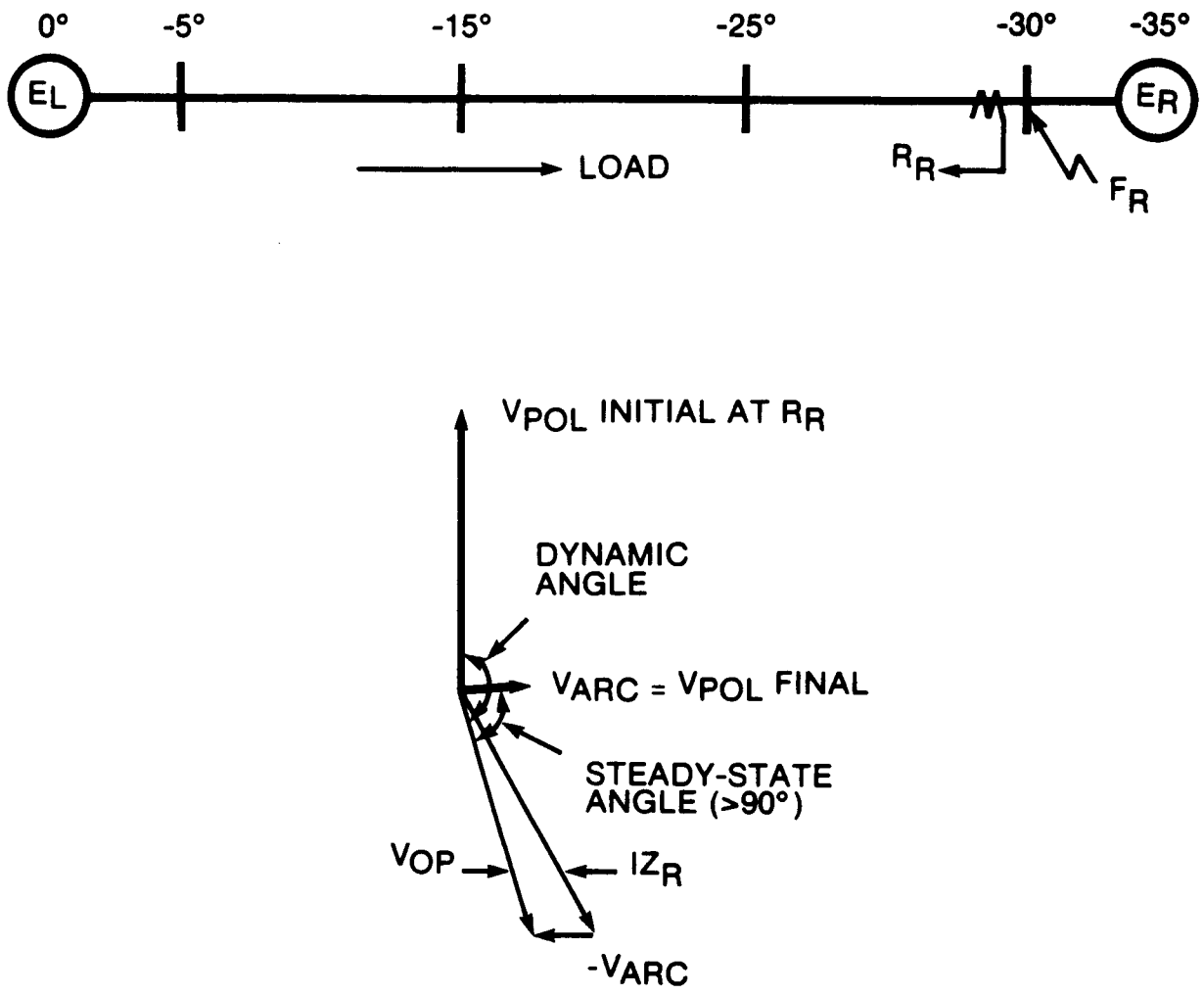


Figure 7. Phasors for R_R Relay and F_R Fault, Load Flow in Non-Tripping Direction

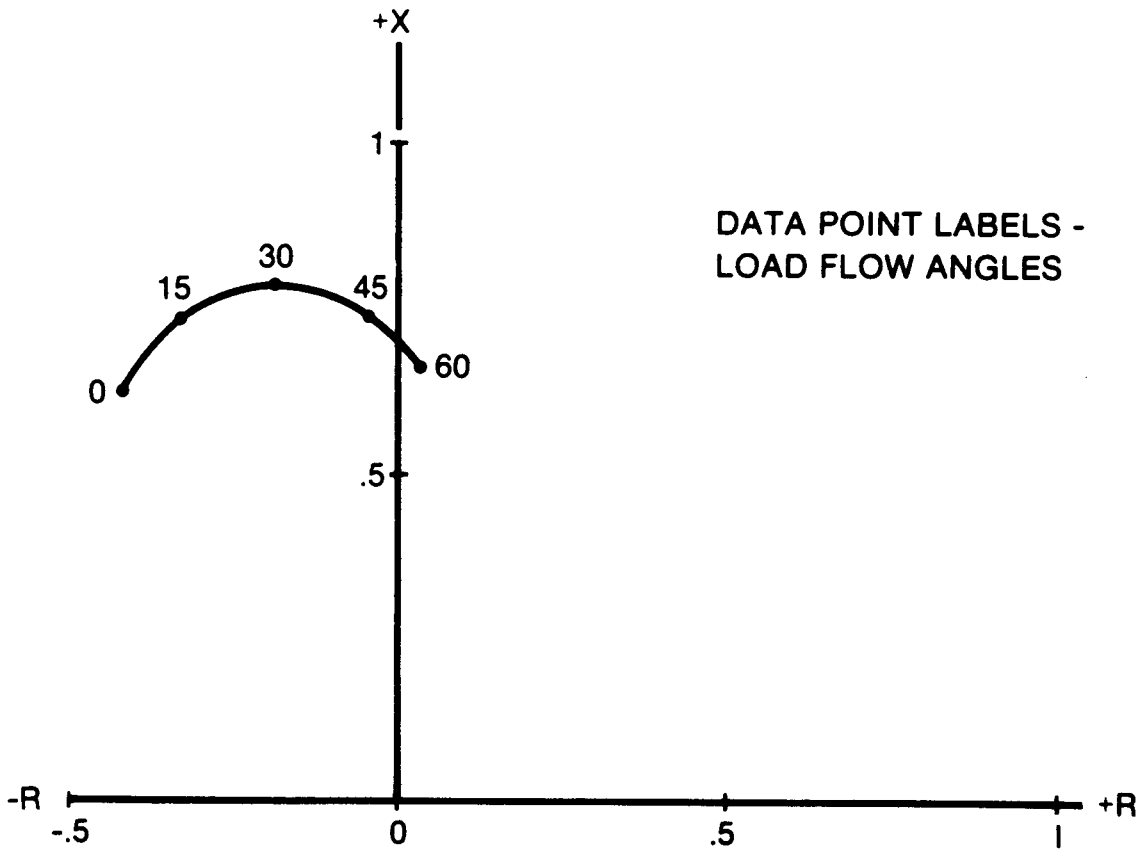


Figure 8. Compensated Impedance Seen by Phase C Relay for A-G Fault at Relay Location

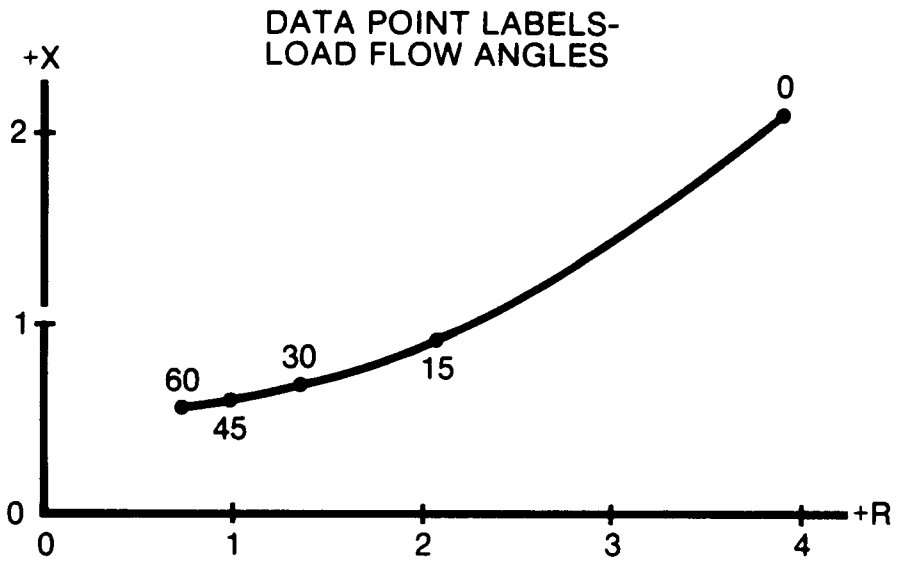


Figure 9. Compensated Impedance Seen by Phase C Relay for A-G Fault at Line-End

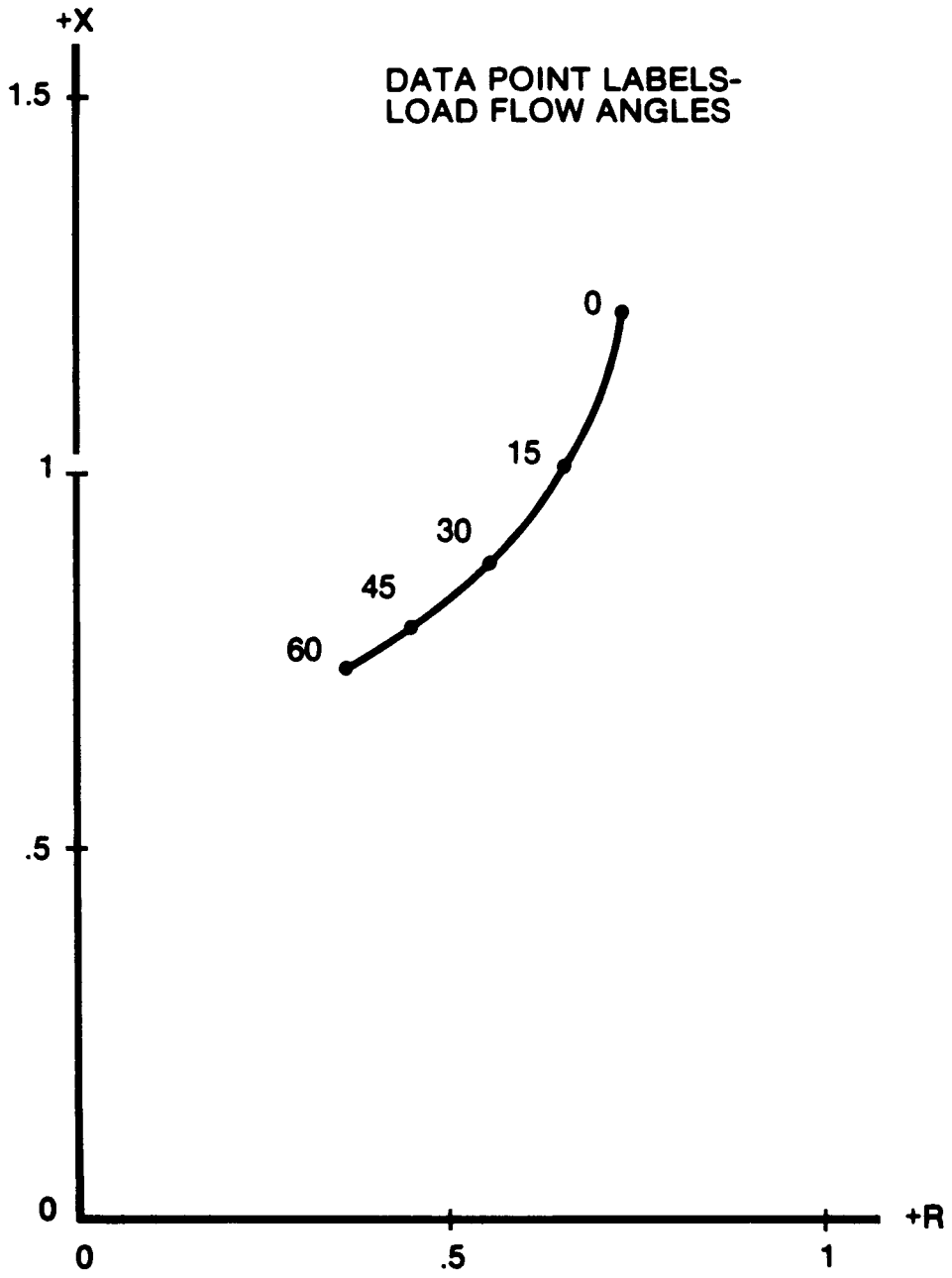


Figure 10. Impedance Seen by Phase C-A Relay for A-G Fault at Line-End

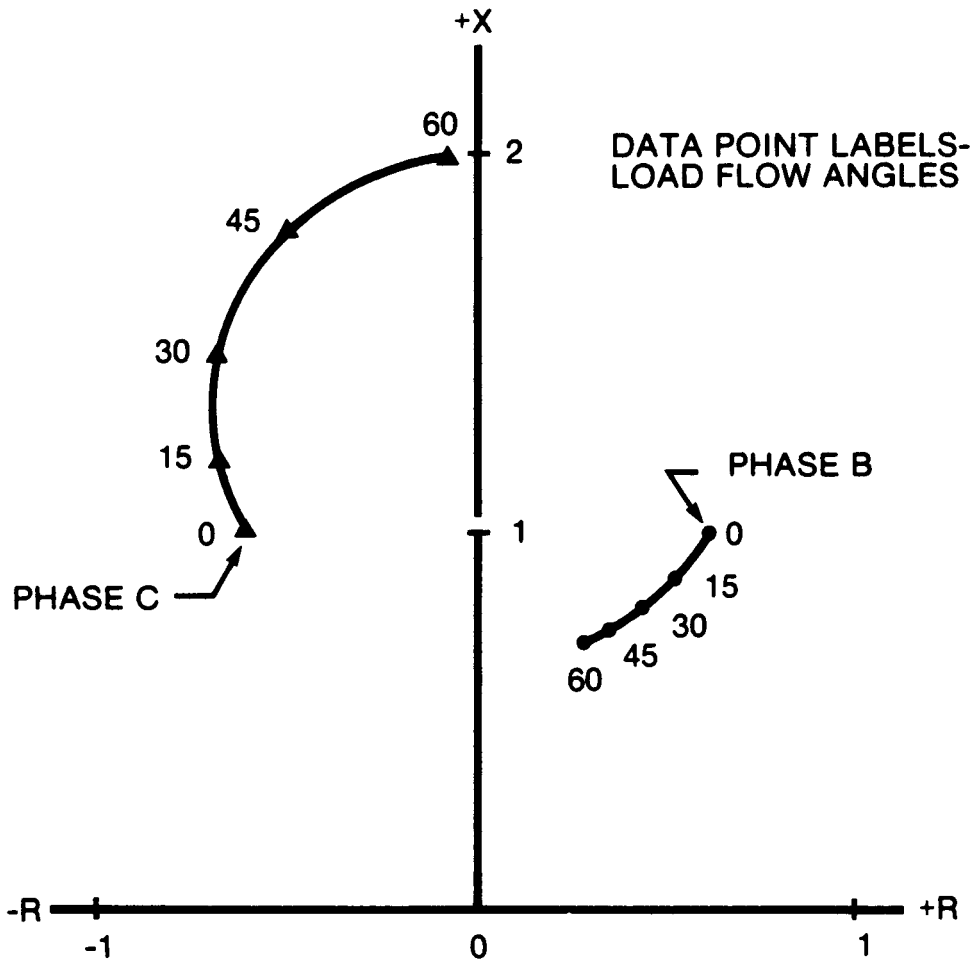


Figure 11. Compensated Impedance Seen by Phase B and Phase C Relay for B-C Fault at Line-End

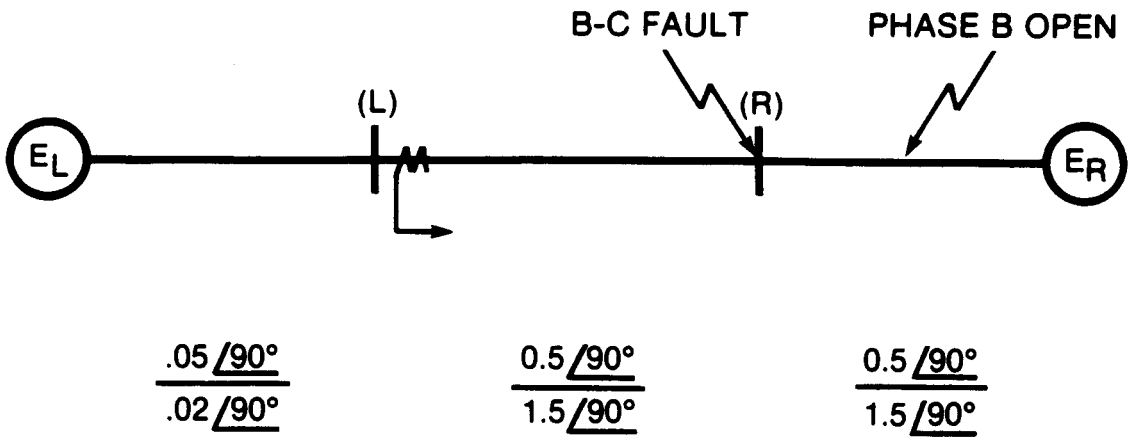


Figure 12. System to Evaluate Performance with One Pole Open

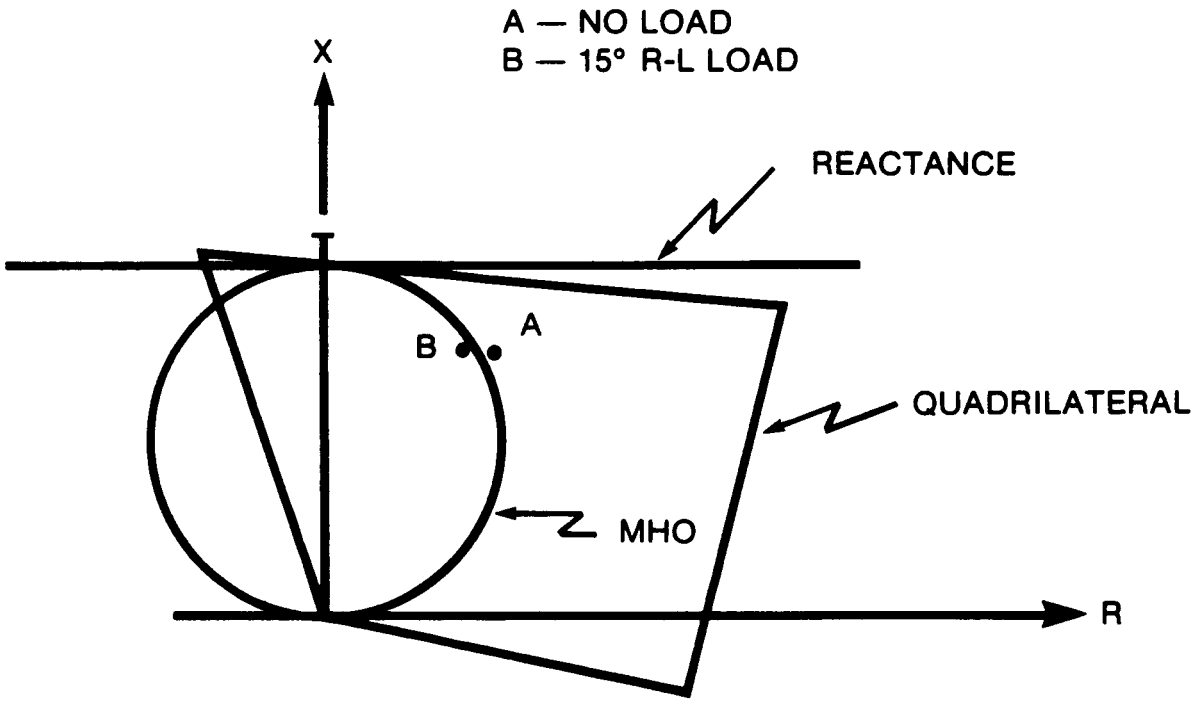


Figure 13. Compensated Impedance Seen by Phase B Relay for B-C Fault at Line-End

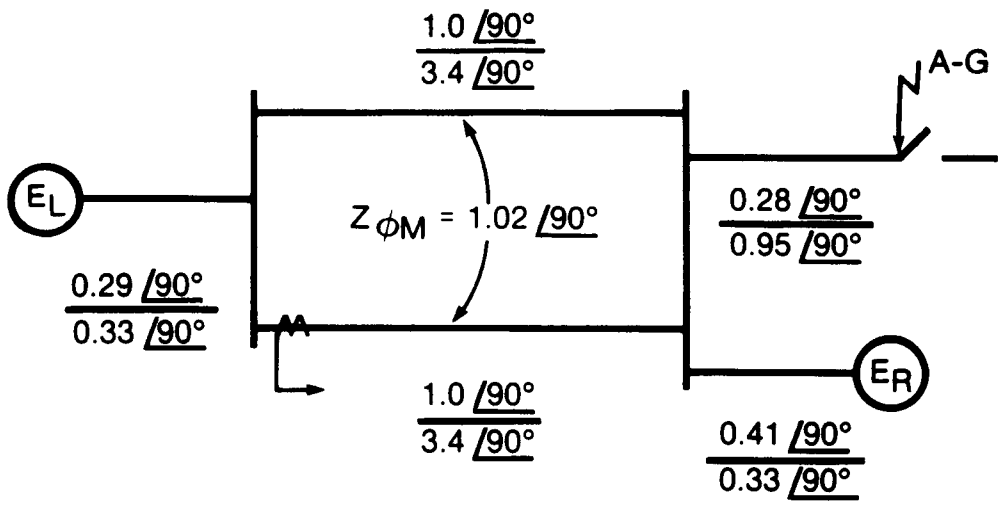


Figure 14(a). System to Evaluate Performance with Fault beyond Remote-End

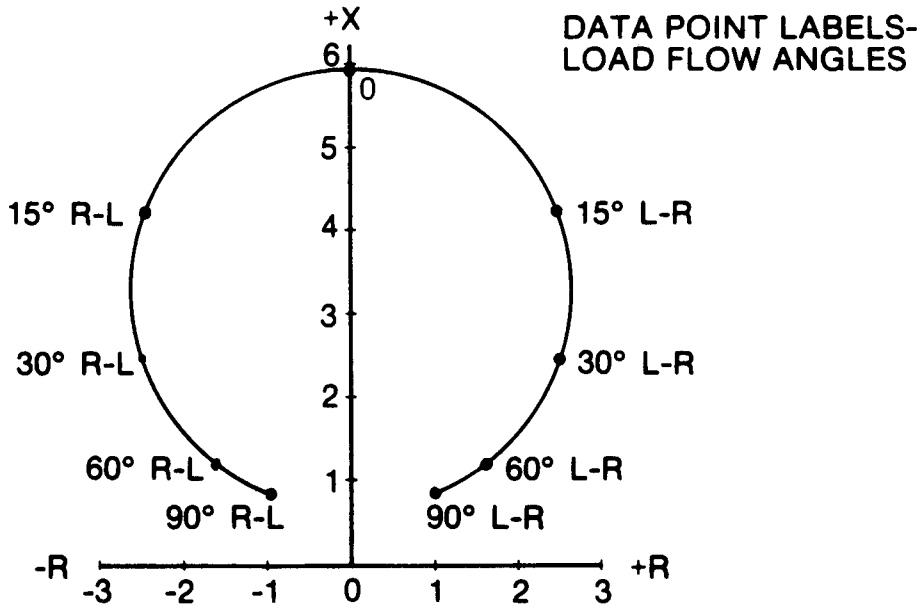


Figure 14(b). Compensated Impedance Seen by Phase A Relay for External A-G Fault

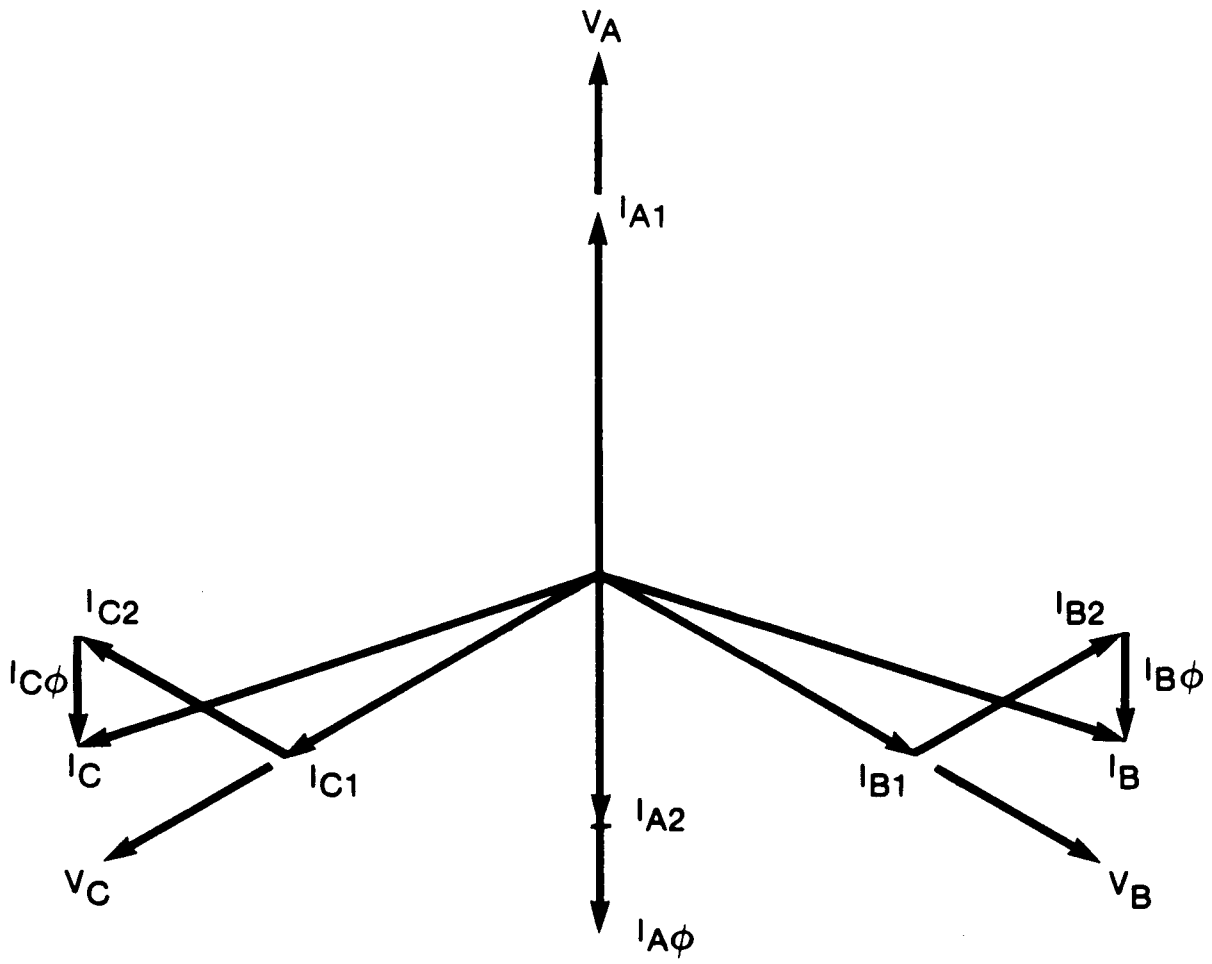


Figure 15. Phasor Diagram with Phase A Open—Dissymmetry Due to $I_2 > I_0$

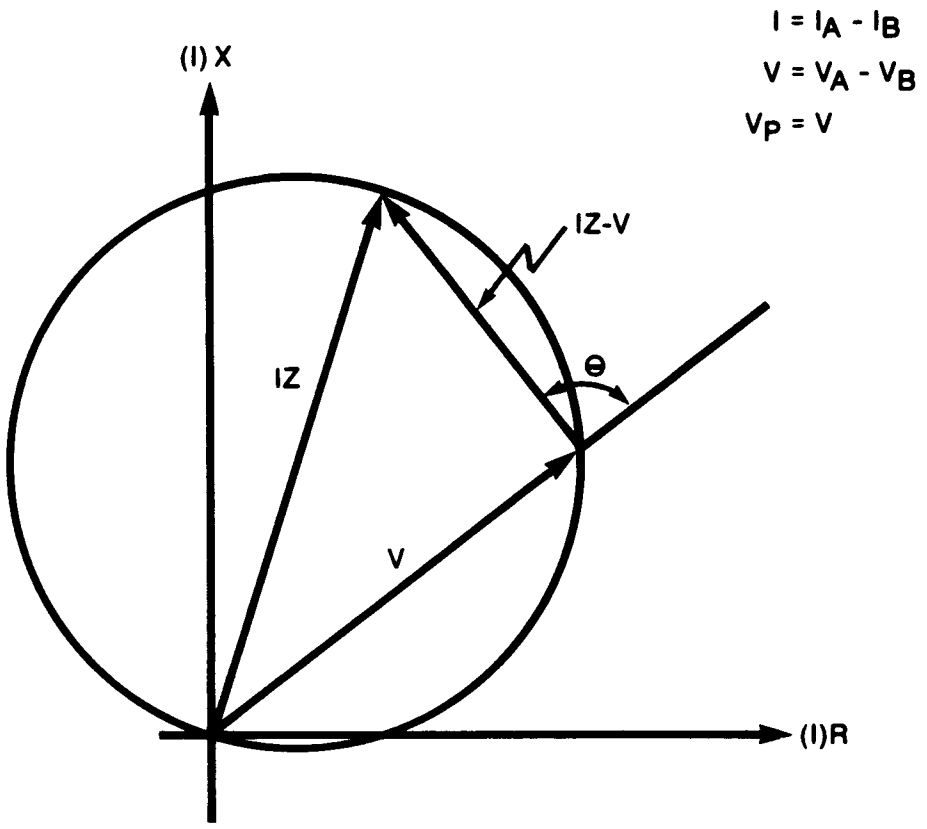


Figure 16. Operate and Polarize Phasors for Phase Mho Unit Plotted on (I)R - (I)X Diagram

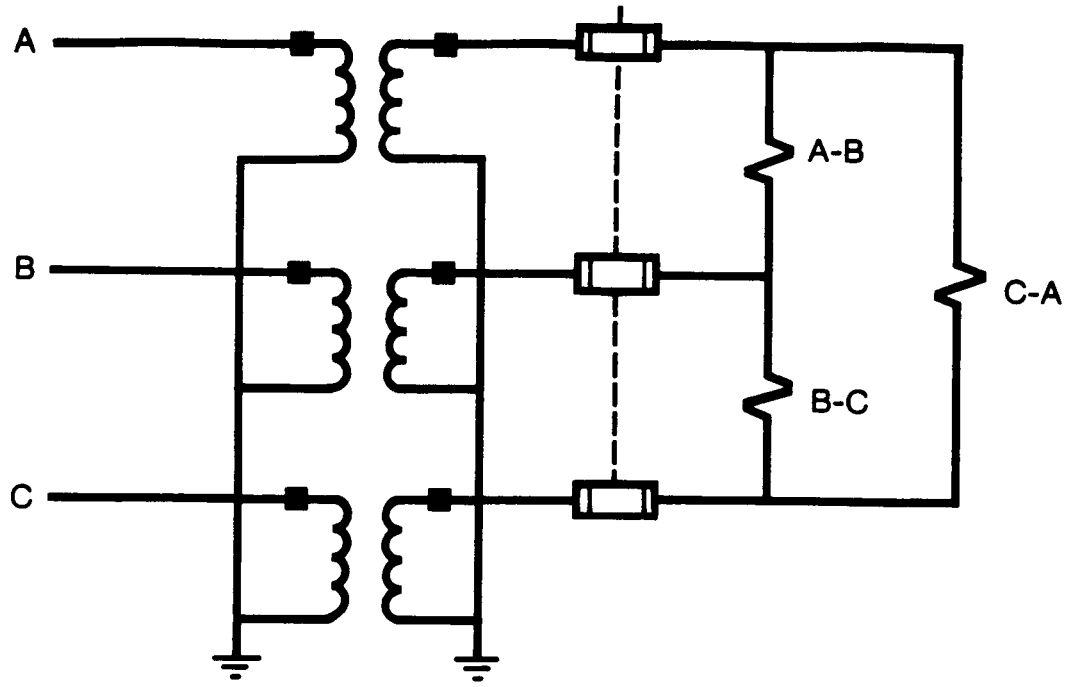


Figure 17. PT Connections

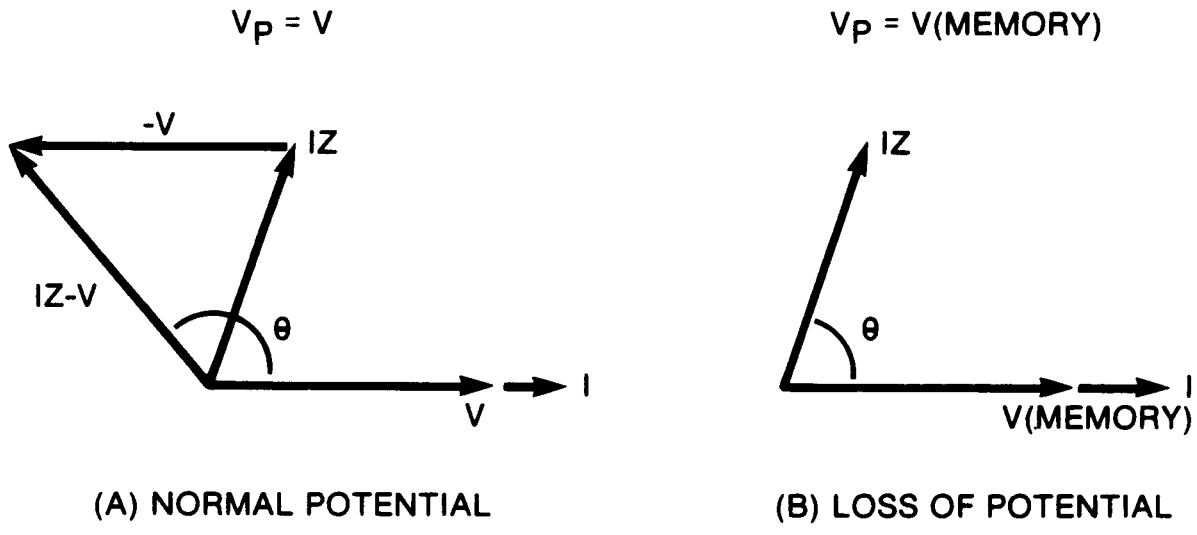
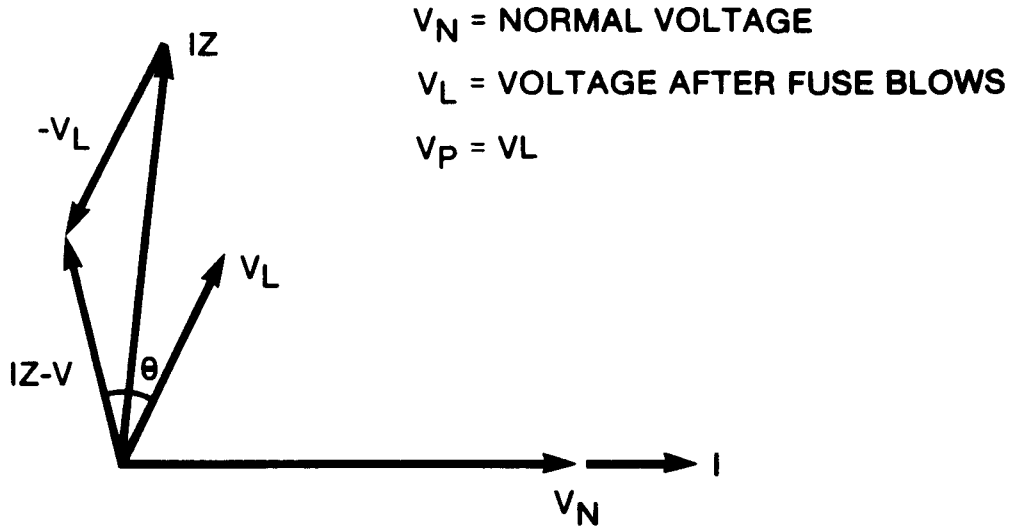
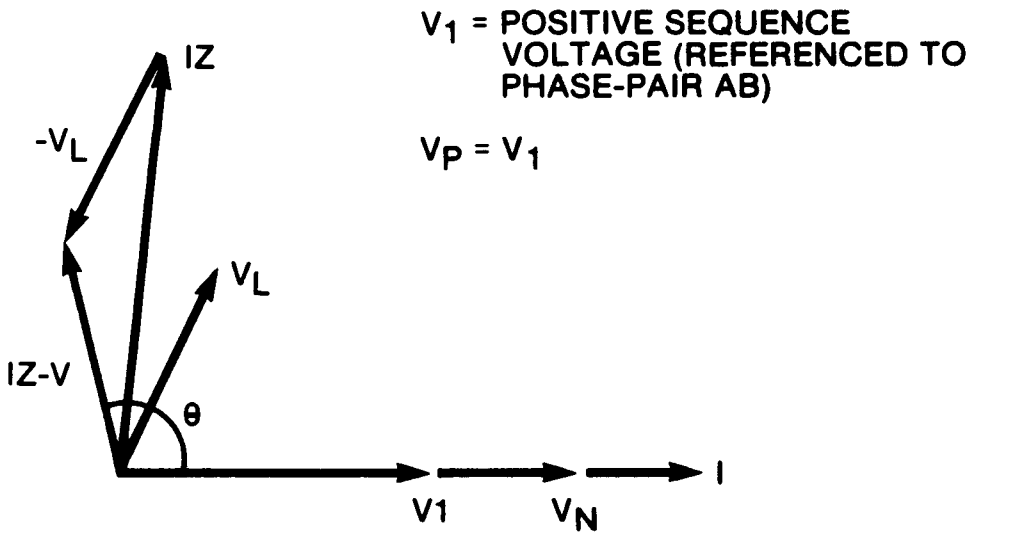


Figure 18. Phasor Diagrams for Normal Potential and Loss of All Potential



(A) PHASE—PAIR VOLTAGE POLARIZATION



(B) POSITIVE SEQUENCE VOLTAGE POLARIZATION

Figure 19. Phasor Diagrams for Blown Fuse in Phase A

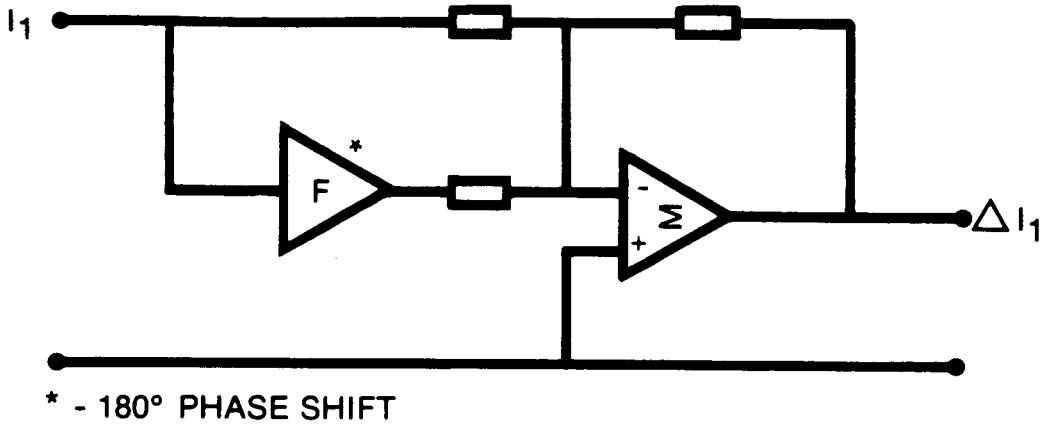


Figure 20. Simplified "Load Memory" Circuit

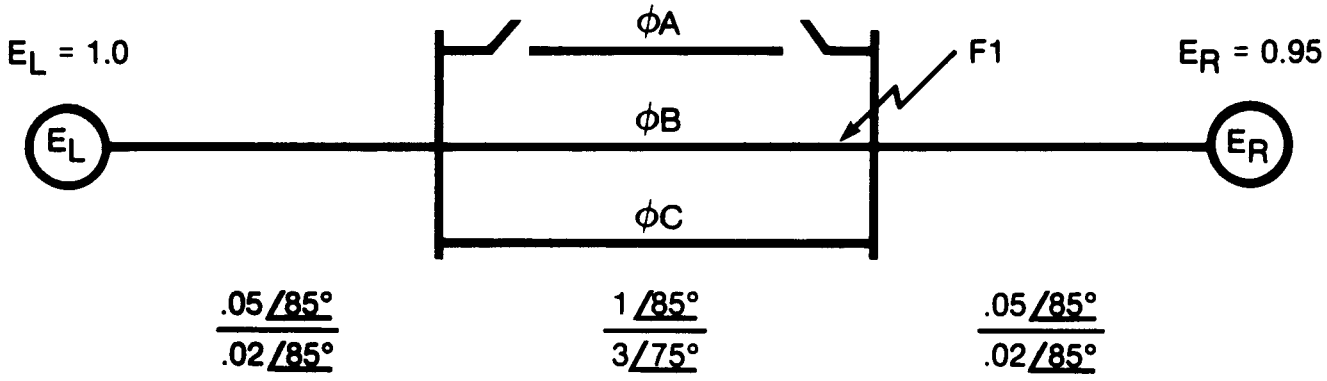


Figure 21. System to Evaluate Performance of Negative and Zero Sequence Directional Overcurrent Relays